

**Remarks**

Claims 11-13, 17 and 45-54 are pending in the application, and were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. More specifically, the use of the phrase "...one or more dielectric layers comprised of latex; and one or more layers of electrically conductive material..." in claims 11 and 17 is asserted to be unclear.

In response, Applicants have amended claim 11 to recite:

"11. An electrical circuit comprised of:

*at least one dielectric layer comprised of latex; and*

*at least a corresponding number of layers of electrically conductive material patterned to form multiple electrical interconnects, at least one of the corresponding number of electrically conductive material layers disposed above a corresponding one of the at least one dielectric layer.*

The Action states that if there were only one dielectric layer, it would be unclear how one dielectric layer would support a plurality of electrically conductive material layers. Clarification of this matter is provided in the discussion with respect to claim 17 below. The amendment further clarifies that the claimed invention envisions at least one conductive layer corresponding to each dielectric layer in the electrical circuit. Applicants respectfully submit that this amendment removes the basis of this rejection, and requests reconsideration and withdrawal thereof.

A similar change has been made to claim 17, which is directed to a multichip module.

The Action states that claims 11 and 17 are unclear because they disclose more than one layer of dielectric layer. Support for one or more than one dielectric layer in an electrical circuit or multichip module finds support in the specification in paragraph [0117], where it is described that the steps for forming a single dielectric layer/conductive material layer will readily be understood to those of ordinary skill in photolithographic art as repeatable to produce additional layers of dielectric and conductive material layers.

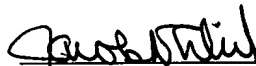
The Action points to Figure 38 and states that it is unclear how one layer of electrically conductive material is able to accomplish the connections recited in claim 17. Applicants indicate the discussion that appears on paragraphs [0110-0113] teaches such connections. The embodiment depicted in Figure 38 includes an additional, thicker layer of electrically conductive material (e.g., copper) deposited by electroplating on a first conductive layer, but, as clearly stated in paragraph [0113], it would be possible to form a single conductive layer entirely by electroless deposition that can serve to form the interconnects recited in claim 17, as amended. Thus, the claim has been amended to reflect that one or more conductive layers may be disposed above each dielectric layer in the multichip module.

Since the 35 USC §112 rejections of claims 11 and 17 are overcome, and there are no rejections based on art, Applicants respectfully state that claims 11 and 17 are clearly allowable. Further, since the other pending rejected claims depend from the allowable claims 11 or 17, as amended, Applicants respectfully submit that all the dependent claims are similarly allowable. For at least the above noted reasons, Applicants respectfully submit that claims 11-13, 17 and 45-54, as amended, are in a condition for allowance, and respectfully requests that the Examiner reconsider and withdraw all outstanding rejections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, please call Applicant's attorney at 617-854-4000.

Respectfully submitted,  
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Dated: September 29, 2003

By:

  
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